Abstract

Please amended the abstract as follows:

Register adjustment is performed based on adjustment values determined at multiple stages within a pipeline of a processor. In one embodiment, a programmable processor is adapted to include a speculative count register. The speculative count register may be loaded with data associated with an instruction before the instruction commits. However, if the instruction is terminated before it commits, the speculative count register may be adjusted. A set of counters may monitor the difference between the speculative count register and its architectural counterpart.